

CLAIMS

What is claimed is:

*Sub 1
BD* and

1. An apparatus, comprising:
a plurality of bond pads configured in an array;
a first plurality of driver cells located to the outside of the plurality of bond pads;
a second plurality of driver cells located to the inside of the plurality of bond pads.
2. The apparatus of claim 1, wherein the plurality of bond pads are configured in a staggered array.
3. The apparatus of claim 2, further comprising a plurality of pre-drive cells located to the inside of the second plurality of driver cells.
4. The apparatus of claim 3, wherein the plurality of bond pads are configured in a staggered array including an inner ring and an outer ring of bond pads.
5. The apparatus of claim 4, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.
6. The apparatus of claim 5, further comprising a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects.

7. The apparatus of claim 6, each the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections.

8. The apparatus of claim 7, the first and second pluralities of driver cells each having a width of approximately 80 microns.

9. A semiconductor device, comprising:
a die including
a plurality of bond pads configured in an array;
a first plurality of driver cells located to the outside of the plurality of bond pads, and
a second plurality of driver cells located to the inside of the plurality of bond pads; and
a lead frame including a plurality of lead fingers, the plurality of lead fingers coupled to the plurality of bond pads by a plurality of bond wires.

10. The semiconductor device of claim 9, wherein the plurality of bond pads are configured in a staggered array.

11. The semiconductor device of claim 10, further comprising a plurality of pre-drive cells located to the inside of the second plurality of driver cells.

12. The semiconductor device of claim 11, wherein the plurality of bond pads are configured in a staggered array including an inner ring and an outer ring of bond pads.

13. The semiconductor device of claim 12, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

14. The semiconductor device of claim 13, further comprising a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects.

15. The semiconductor device of claim 14, each the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections.

16. The semiconductor device of claim 15, the first and second pluralities of driver cells each having a width of approximately 80 microns.

17. A method, comprising:

configuring a plurality of bond pads on a die in an array;

placing a first plurality of driver cells to the outside of the plurality bond pads; and placing a second plurality of driver cells to the inside of the plurality of bond pads.

18. The method of claim 17, wherein configuring the plurality of bond pads in an array includes configuring the plurality of bond pads in a staggered array.

19. The method of claim 18, further comprising placing a plurality of pre-driver cells to the inside of the plurality of bond pads.

20. The method of claim 19, further comprising electrically coupling each of the plurality of pre-driver cells to one of the first and second plurality of driver cells.

21. The method of claim 20, further comprising connecting each of the plurality of bond pads to one of a plurality of lead fingers on a lead frame.